Recovery of Random Telegraph Noises in a Stacked CMOS Image Sensor by High-Temperature Annealing after Hot-Carrier Stress

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***Abstract*—**In this paper we first study the temperature effects on the device aging, in particular the random telegraph noise (RTN) degradation and the threshold voltage (V_t) shift in a stacked CMOS image sensor (CIS) caused by hot-carrier stress (HCS). The measured data show both are worse when stressed at lower temperatures (–35°C). Furthermore, we find that the RTN traps generated by HCS can be annealed effectively by a subsequent high temperature bake at 240°C for up to 360 min. In contrast, the RTN traps in chips not stressed by hot carriers are mostly unaffected by annealing at 240°C for the same amount of time. The results suggest that the physical structure of the RTN traps caused by process induced damage (PID) without HCS might be different from those created by HCS. The exact microscopic nature of the differences between these two kinds of RTN traps are not clear at this time and requires further investigation.

I. Introduction

Device aging and reliability issues are important for all semiconductor products, and CIS is no exception. Several known aging mechanisms include the hot carrier injection (HCI), the bias temperature instability (BTI), the time dependent dielectric breakdown (TDDB), and the electron migration (EM). In this work we focus on the HCI effects.

As the CIS pixel pitch continues to shrink, it becomes increasingly challenging to maintain a high full-well capacity while keeping the readout noises low to ensure a good signal-to-noise ratio. The RTN is one of the major contributors to low-frequency noises [1], which is generally believed to be caused by PID.

Previously we reported the degradation of RTN caused by hot-carrier stress (HCS) in a stacked CIS at room temperature and the notable difference from the V_t shift [2]. In this study, the HCS temperatures cover a wider range from –35°C to 120°C. Further, we investigate the effects of high temperature anneal (240°C) on RTN after the HCS. By analyzing the time-domain noise waveform of each pixel in an 8.3 MP array, we could sort all pixels into two categories: the RTN-like and non-RTN. Then, we monitor the changes of each pixel's noise behavior through a series of stress and anneal experiments.

II. Test Chip Characteristics

The test chip is a stacked CIS with the top pixel layer fabricated by a 28 nm 1P4M CIS process and the bottom layer readout circuits by a 22 nm 1P7M mixed-mode process. The array consists of $2512^{V}\times3296^{H}$ (8.3M) pixels of a 0.8 um pitch and a 4×2 shared structure, read out by 1648 12-bit column ADCs with front amplifiers supporting 1X to 8X analog gains. A simplified chip architecture is shown in Fig. 1. The three pixel-devices (RST, RSL, SF) can be operated up to 3.3 V. The device under test (DUT) is the source follower (SF) NMOS with W = 0.16 um, L = 0.87 um, and 5.7 nm dielectric thickness, biased by a constant current source of 7.2 uA in normal operations. The conversion factor from the ADC output to the SF input is 292 uV/DN at 1X gain and 36.5 uV/DN at 8X gain. The median read noise is about 190 uV-rms operated at 60 MHz clock and 1.48 fps frame rate. The random noise (RN) is measured at 8X gain while the V_t shift is measured at 1X gain, calculated back to input-referred values at the SF gates. In SF testing mode the transfer gates (TG) are disabled so that the photon shot noises are not involved.

III. Temperature Effect of Hot Carrier Stress

The SF drain voltage ($V_d = V_{PIX}$) in Fig. 1 is set to 3.1 V for normal operations. When V_{PIX} is increased, the channel conduction electrons are accelerated by the lateral electric field and gain kinetic energies. The energetic (hot) electrons can in turn generate more electron-hole pairs via impact ionization, manifested as the rapid increase of the substrate current due to the holes. When the electron energy exceeds the electron affinity difference between Si and SiO_2 (about 3.25 eV), it can jump over the Si-SiO_2 barrier or tunnel through the barrier to damage the oxide. In Fig.1 bias setup, the SF source voltage (V_s) is about 1.5 V. A significant substrate current increase is observed when V_{PIX} exceeds 5.5 V when the SF V_{DS} is higher than 4 V.

In this study the V_{PIX} is raised to 6.0 V to accelerate HCS aging. The damage caused by HCI can be characterized as the V_t shift and the RTN degradation [2]. Figs. 2–3 show the measured changes of RTN and V_t shift at the distribution tail (ICDF = 10^{-5}) as a function of stress time from 10 min to 780 min. Figs. 4–5 show the degradation of RTN and V_t shift stressed under different temperatures (–35°C to 120°C) for a same stress time (380 min) at various ICDF levels. It is clear that the HCS can cause larger device degradation at lower temperatures. This is consistent with reports in literature [3–5] for long channel (approx. > 100 nm) devices. It is also known that the temperature trend is opposite for short channel (< 100 nm) devices [6–7] due to different mechanisms. The DUT in this work has a channel length of 870 nm; therefore, is a long channel device. The data in Fig. 6 verify that the substrate currents I_B measured from a same size device on separated test keys are indeed higher at lower temperatures, consistent with the known trend of the degradation.

IV. Recovery by High Temperature Anneal

After HCS, the next is to find out how the device degradation can be reversed by high temperature anneal. We experimented with a range from 60°C to 240°C and a anneal time range from 10 min to 360 min. For the rest of the paper, we only discuss the results of a constant –35°C stress followed by a constant 240°C anneal. All the measurements were performed when the chips reach equilibrium with room temperature. Figs. 7(a)–(b) show a family of RN distribution curves after stressed from 10 min to 780 min. Figs. 8(a)–(b) show the reversed trend of RN recovery by a 240°C anneal from 10 min to 360 min. It is apparent that the device suffers considerable damage at the end of the stress but recovers almost completely after the anneal. Figs. 9(a)–(c) show that the RTN degradation does not happen uniformly to all pixels. The pixels on the lower right branch of the 2D correlation plot Fig. 9(b) suffer a higher degradation while the pixels around the $x = y$ diagonal line remain largely unchanged. The corresponding V_t shifts are plotted in Figs. 10–12 similarly for comparison. As pointed out in [2], the striking difference between the RTN degradation and V_t shift is that the V_t shift occurs to all pixels relatively uniformly, contrary to the discrete nature of RTN degradation. The similarities between Figs. 7–9 and Figs. 10–12 are that the stress induced damages are recoverable after elevated temperature anneal.

V. Key Findings and Discussions

The typical RN distributions are non-Gaussian and highly skewed with long tails where the RTN pixels are usually found. There is no clear border in the distributions separating the RTN and the non-RTN pixels. The only way we know of to identify a RTN pixel is to examine its time-domain noise waveforms. The DUTs with noise histograms showing discrete levels or deviating significantly from Gaussian are classified as RTN and RTN-like [2,8]. The rest DUTs are considered as non-RTN pixels. Figs. 13(a)–(c) are the sorting results of before stress, after stress, and after annealing, respectively, where N_0 is the total number of devices (about 1M SF's out of the 8M array), N_1 is the non-RTN devices, and N_2 is the RTN-like devices, including N_3 showing 2 discrete RTN levels and N_4 showing 3 or more levels. The key finding is that the total RTN-like devices are increased dramatically from 5.2k (0.52%) to 31k (3.1%) after HCS and reduced to 6.7k (0.67%) after annealing. The numbers are summarized in Table 1 for comparison.

A detailed breakdown in Table 2 further illustrates how the non-RTN devices change into RTN-like and vice versa from the initial condition before stress to the end of 780 min stress at –35°C and then after the 210 min anneal at 240°C.

One highlight is that 28,388 devices were originally non-RTN before stress but turned into RTN-like after stress. Subsequently, about 98% of them (27,856) recovered back to non-RTN after the annealing.

In contrast, the percentage of RTN-like devices of un-stressed chips are mostly unchanged after the anneal at 240°C for the same duration of time. This may be explained by the fact that the RTN traps are likely generated in the front-end-of-line (FEOL) fabrication process by PID such as the high energy implantation and reactive ion etching. During the back-end-of-line (BEOL) process the wafers are typically subject to annealing at temperatures higher than 240°C for longer than a few hours. In other words, the traps that can be annealed have already been eliminated.

This observation suggests that there are two kinds of RTN traps. The RTN traps at the time of fab-out have survived the high temperature treatment in the BEOL process; therefore, cannot be annealed further. They may be tentatively called the "hard" RTN traps. On the other hand, the HCS generates many new "soft" RTN traps which can be easily eliminated by subsequent high temperature anneal. This important distinction among different RTN traps was not pointed out in the literature before to the best of our knowledge.

Several studies have linked the HCI induced interface states and oxide traps to the dissociation of Si-H bonds which create Si dangling bonds. Reversely, the annealing of the traps by high temperature could be explained by the hydrogen re-passivating the Si dangling bonds [7,9–16]. The nominal Si-H bond strength is about 3.6 eV; however, some reports showed that the Si-H bond can be broken by hot electrons of energies much less than 3.6 eV [14–15].

The defects in bulk SiO_2 and on the Si-SiO_2 interface have many complicated forms such as vacancies, interstitials, Si dangling bonds (P_b centers), oxygen vacancies (E' centers), peroxyl radicals, and the non-bridging oxygen hole centers [17–19]. The electronic excitation or charge trapping on some of these sites may alter their atomic configurations. It might be possible that the differences between the hard RTN and soft RTN traps are related to the atomic structural differences of the traps, although our macroscopic data cannot lead to any specific microscopic pictures.

VI. Conclusion

We pointed out one key difference between the native or built-in RTN traps in samples unstressed after fab out and the RTN traps caused by hot carrier stress. The latter can be mostly eliminated by a 240°C anneal in room air for a few hours while the former cannot be annealed. The underlying physics is not clarified yet. We hope this study could stimulate further investigations, perhaps by atomic structure modeling, calculation, and simulation.

VII. Reference

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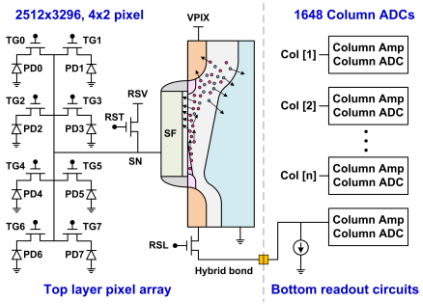

Fig. 1. Simplified architecture of the 8.3 MP, 0.8 um pitch stacked CIS. The devices under hot-carrier stress are the source followers (SF) in the 4x2-shared pixel groups on the top layer. The total number of SF is 628x1648.

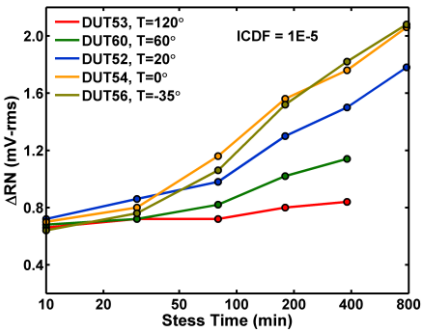

Fig. 2. Random noise degradation (ΔRN) at the distribution tail (ICDF = 1E-5) as a function of the time of hot-carrier stress at temperatures from –35°C to 120°C.

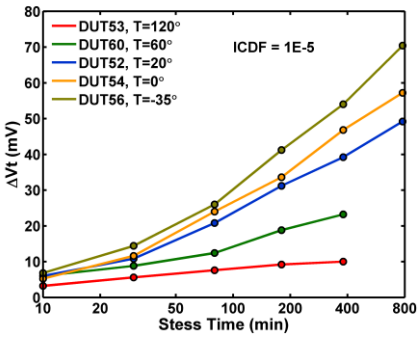

Fig. 3. SF threshold voltage shift (ΔVt) at the distribution tail (ICDF = 1E-5) as a function of the time of hot-carrier stress at temperatures from –35°C to 120°C.

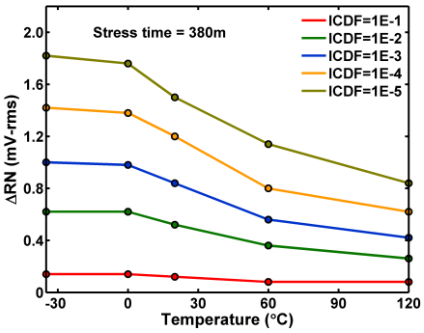

Fig. 4. Temperature dependence of the random noise degradation (ΔRN) after 380 min hot-carrier stress at various constant-ICDF contours.

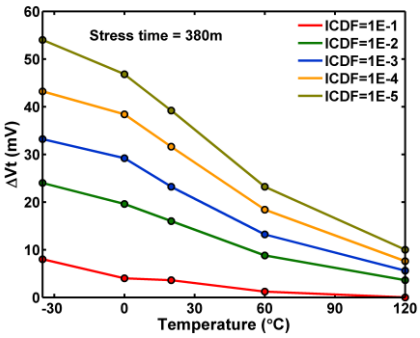

Fig. 5. Temperature dependence of the SF threshold voltage shift (ΔVt) after 380 min hot-carrier stress at various constant-ICDF contours.

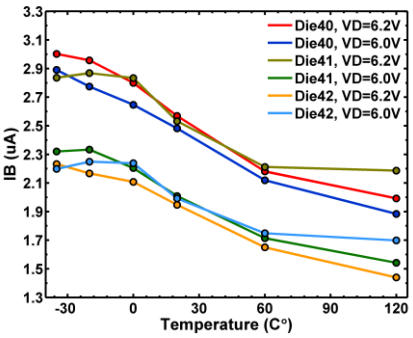

Fig. 6. Temperature dependence of the substrate current (I_B) of the SF devices on separate test keys biased by a constant current I_S = 7.2uA, V_D = 6.0V and 6.2V.

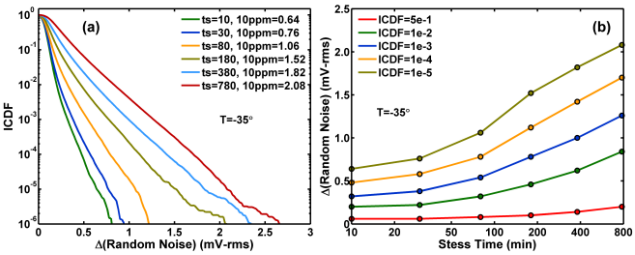

Fig. 7. (a) A family of ICDF curves of the random noise degradation (ΔRN) stressed by hot-carrier injection at –35°C for a duration from 10 min to 780 min. (b) A family of constant-ICDF contours as functions of the stress time.

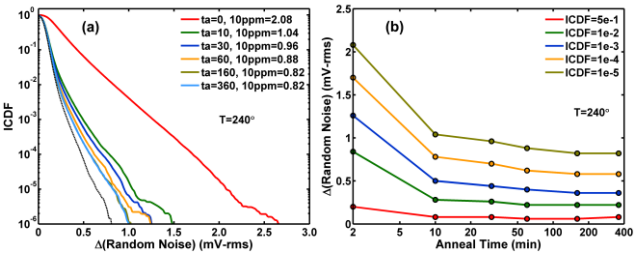

Fig. 8. (a) A family of ICDF curves of the random noise degradation (ΔRN) recovered by high-temperature anneal at 240°C for a duration from 10 min to 360 min, where the dark-gray dash curve is the ICDF before stress. (b) A family of constant-ICDF contours as functions of the annealing time.

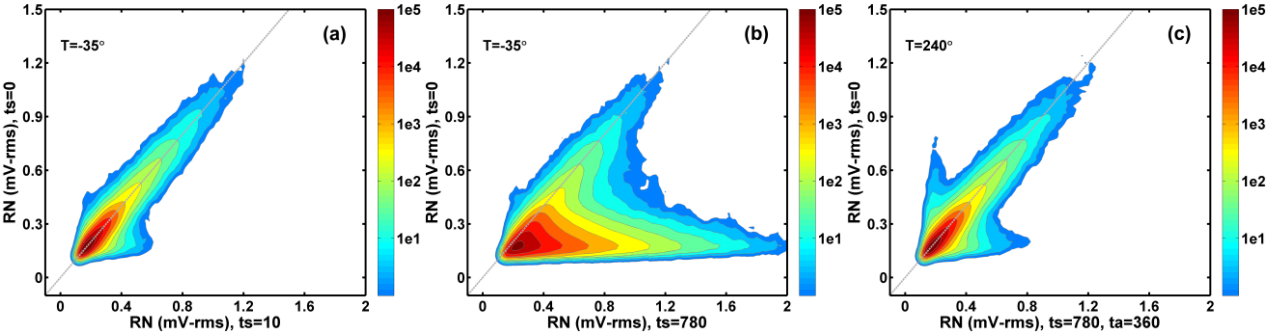

Fig. 9. The 2D histograms of the correlations of the random noises (RN) before hot-carrier stress, after hot-carrier stress at –35°C, and after high-temperature anneal at 240°C. (a) The RN after 10 min stress compared to the RN before stress. (b) The RN after 780 min stress compared to the RN before stress. The devices on the lower right branch of the 2D histogram show a dramatic increase of RN after stress. A majority of them are RTN-like devices. (c) The RN after 360 min annealing at 240°C vs. the RN before stress. It shows that most of the RN degradation recovered after the 240°C anneal.

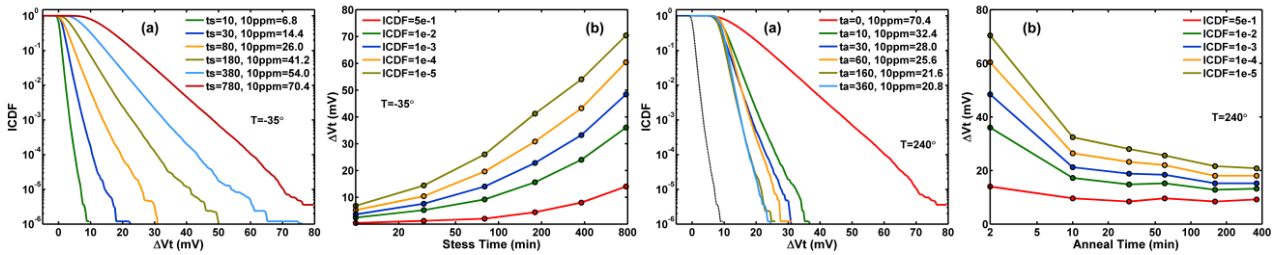

Fig. 10. (a) A family of ICDF curves of the threshold voltage shift (ΔVt) stressed by hot-carrier injection at –35°C for a duration from 10 min to 780 min. (b) A family of constant-ICDF contours as functions of the stress time.

Fig. 11. (a) A family of ICDF curves of the threshold voltage shift (ΔVt) recovered by high-temperature anneal at 240°C for a duration from 10 min to 360 min, where the dark-gray dash curve is the ICDF before stress. (b) A family of constant-ICDF contours as functions of the anneal time.

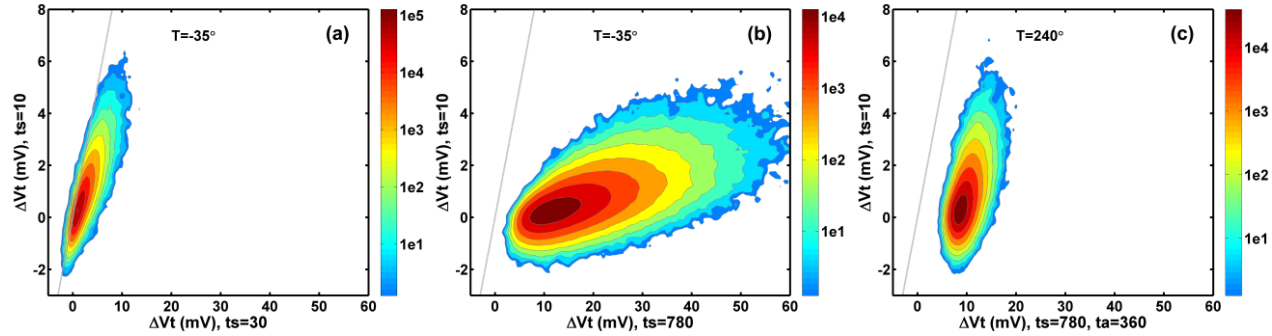

Fig. 12. The 2D histograms of the correlations of the threshold voltage shift (ΔVt) before hot-carrier stress, after hot-carrier stress at –35°C, and after annealing at 240°C. (a) The ΔVt after 10 min stress compared to the ΔVt before stress. (b) The ΔVt after 780 min stress vs. the ΔVt before stress. All the devices show systematic increases of ΔVt after stress. The light-gray dash line is the X=Y reference line. (c) The ΔVt after 360 min annealing at 240°C vs. the ΔVt before stress. It shows that a substantial portion of the ΔVt degradation recovered after the 240°C anneal. However, a visible parallel shift from the X=Y reference line suggests that a uniform increase of ΔVt among all devices still remain, although the spread of ΔVt almost returns to the pre-stress condition.

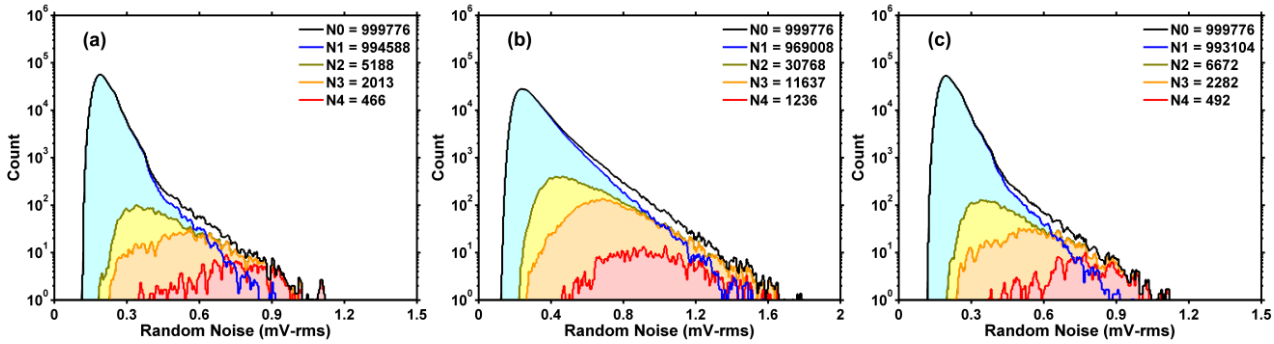

Fig. 13. The RN distributions (a) before the stress; (b) after the stress at –35°C for 780 min; and (c) after the anneal at 240°C for 210 min. The total number of devices (N_0) is about 1M, sorted into 4 sub-groups where N_1 is the number of non-RTN devices and N_2 is the RTN-like devices ($N_0 = N_1 + N_2$). The numbers of devices with noise distribution showing more than 2 or 3 discrete levels are N_3 and N_4, respectively. The RTN-like devices (N_2) include the devices with noise distributions significantly deviating from the Gaussian distributions, in addition to those showing multiple discrete levels. The key observation is that the number of RTN-like device increases dramatically after stress but decreases almost to the initial number after annealing.

RN Types	Before Stress	After Stress	After Anneal
3 or more levels (N_4)	466	1,236	496
2 or more levels (N_3)	2,013	11,637	2,282
RTN-like (N_2)	5,188	30,768	6,672
Non-RTN (N_1)	994,588	969,008	993,104
Total (N_0)	999,776	999,776	999,776

Table 1. Summary of the number of devices in each sub-groups (N_0, N_1, N_2, N_3, N_4) before stress, after stress, and after annealing corresponding to the numbers in the RN histograms in Fig. 13 (a), (b), and (c), respectively.

Before Stress		After Stress		After Anneal	
RTN-like (K_1)	5,188	RTN-like (K_{11})	2,380	RTN-like (K_{111})	2,314
				Non-RTN (K_{110})	66
		Non-RTN (K_{10})	2,808	RTN-like (K_{101})	2,047
				Non-RTN (K_{100})	761
Non-RTN (K_0)	974,588	RTN-like (K_{01})	28,388	RTN-like (K_{011})	532
				Non-RTN (K_{010})	27,856
		Non-RTN (K_{00})	946,200	RTN-like (K_{001})	1,779
				Non-RTN (K_{000})	944,421

Table 2. The evolution of the RN behaviors for all devices (either non-RTN or RTN-like) from the initial state before stress, to after stress, and finally after annealing. The highlight is that 28,388 devices changed from non-RTN to RTN-like after stress and 98% of them (27,856) recovered from RTN-like back to non-RTN after high-temperature annealing.